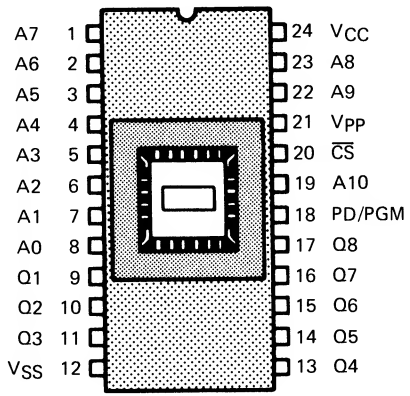
TMS 2516-25 JL, TMS 2516-35 JL AND TMS 2516-45 JL
16,384-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

DECEMBER 1979—REVISED MAY 1982

- Organization . . . 2048 X 8
- Single +5 V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time
  - TMS 2516-25 . . . 250 ns
  - TMS 2516-35 . . . 350 ns
  - TMS 2516-45 . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power
  - Active . . . 285 mW Typical
  - Standby . . . 50 mW Typical
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required

24-PIN CERPAK
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address inputs
$\overline{CS}$	Chip Select
PD/PGM	Power Down/Program
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

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description

The TMS 2516 series are 16,384-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS 2516 is plug-in compatible with the TMS 4016 16K static RAM. It is offered in a dual-in-line cerpak package (JL suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single +5 V supply (in the read mode), they are ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 50-ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 100 seconds.

operation

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming	Program Verification
PD/PGM (18)	V_{IL}	Don't Care	V_{IH}	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IL}
$\overline{CS}$ (20)	V_{IL}	V_{IH}	Don't Care	V_{IH}	V_{IH}	V_{IL}
V_{PP} (21)	+5 V	+5 V	+5 V	+25 V	+25 V	+25 V (or +5 V)
V_{CC} (24)	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
Q (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	HI-Z	Q

read/output disable

When the outputs of two or more TMS 2516's are connected to the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the $\overline{CS}$ and PD/PGM pins. All other devices in the circuit should have their outputs disabled by applying high-level signals to these same pins. PD/PGM can be left low, but it may be advantageous to power down the device during output disable. Output data is accessed at pins Q1 through Q8. On the TMS 2516-45 data can be accessed in 450 ns and access time from $\overline{CS}$ is 150 ns. On the TMS 2516-35 and TMS 2516-25 data can be accessed in 350 and 250 (respectively) and access time from $\overline{CS}$ is 120 ns. These access times assume that the addresses are stable.

power down

Active power dissipation can be cut by 80% by applying a high TTL signal to the PD/PGM pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2516 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity times exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12-milliwatt per-square-centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state (assuming a high-level output corresponds to logic "1").

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0" can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V and $\overline{CS}$ is at V_{IH}. Data is presented in parallel (8 bits) on pins Q1 through Q8. Once addresses and data are stable, a 50-millisecond TTL high-level pulse should be applied to the PGM pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. Several TMS 2516's can be programmed simultaneously when the devices are connected in parallel.

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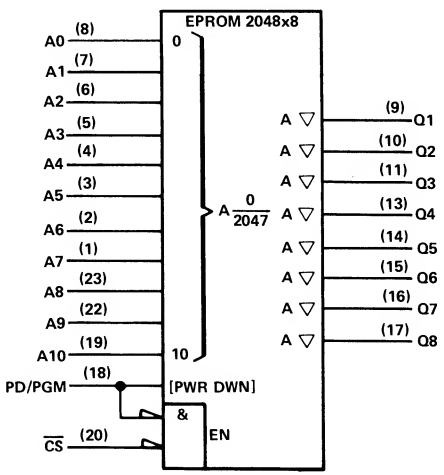
inhibit programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen devices. TMS 2516's not intended to be programmed (i.e., inhibited) should have a low level applied to the PD/PGM pin and a high-level applied to the CS pin

program verification

A verification is done to see if the device was programmed correctly. A verification can be done at any time. It can be done on each location immediately after that location is programmed. To do a verification, V_{PP} may be kept at +25 V.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 289.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . −0.3 to 6 V
Supply voltage, V_{PP} (see Note 1) . . . . . −0.3 to 28 V
All input voltages (see Note 1) . . . . . −0.3 to 6 V
Output voltage (operating with respect to V_{SS}) . . . . . −0.3 to 6 V
Operating free-air temperature range . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −55 °C to 125 °C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{SS} (substrate).

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	TMS 2516-25			TMS 2516-35			TMS 2516-45			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		VCC			V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0			0		V
High-level input voltage, V_{IH}	2	$V_{CC}+1$		2	$V_{CC}+1$		2	$V_{CC}+1$		V
Low-level input voltage, V_{IL}	−0.1		0.8	−0.1		0.8	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$	250			350			450			ns
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC}+I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage*	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage*	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.25 V			10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		10	25	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{CS}$ = PD/PGM = V_{IL}		57	100	mA

† Typical values are at T_A = 25°C and nominal voltage.
* All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

capacitance over recommended supply voltage and operating free-air temperature ranges, f = 1 MHz*

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

†All typical values are T_A = 25°C and nominal voltage
*Capacitive measurements are made on sample basis only

switching characteristics over full ranges of recommended operating conditions (see Note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	TMS 2516-25 MIN	TMS 2516-25 TYP†	TMS 2516-25 MAX	TMS 2516-35 MIN	TMS 2516-35 TYP†	TMS 2516-35 MAX	TMS 2516-45 MIN	TMS 2516-45 TYP†	TMS 2516-45 MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leqslant 20$ ns, $t_f \leqslant 20$ ns		230	250		250	350		280	450	ns
$t_{a(CS)}$	Access time from chip select				120			120			150	ns
$t_{a(PR)}$	Access time from PD/PGM			230	250		250	350		280	450	ns
$t_{v(A)}$	Output data valid after address change		0			0			0			ns
$t_{dis(CS)}$	Output disable time from chip select during read only‡		0		100	0		100	0		100	ns
$t_{dis(CS)}$	Output disable time from chip select during program and program verify‡				120			120			120	ns
$t_{dis(PR)}$	Output disable time from PD/PGM‡		0		100	0		100			100	ns

† All typical values are at T_A = 25°C and nominal voltages.

‡ Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(CS)}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(CS)}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

† Typical values are at nominal voltages.

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and V_{PP} = 25 V ± 1 V during programming. All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(CS)}$, and t_{dis}, PD/PGM = $\overline{CS}$ = V_{IL}.

PARAMETER MEASUREMENT INFORMATION

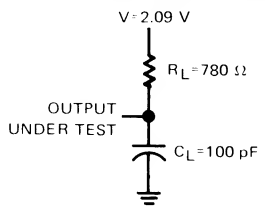
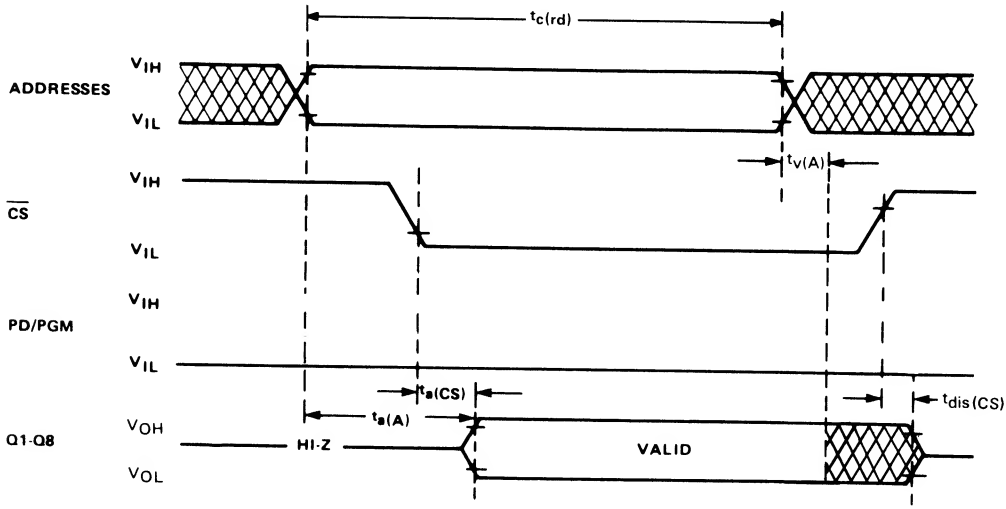
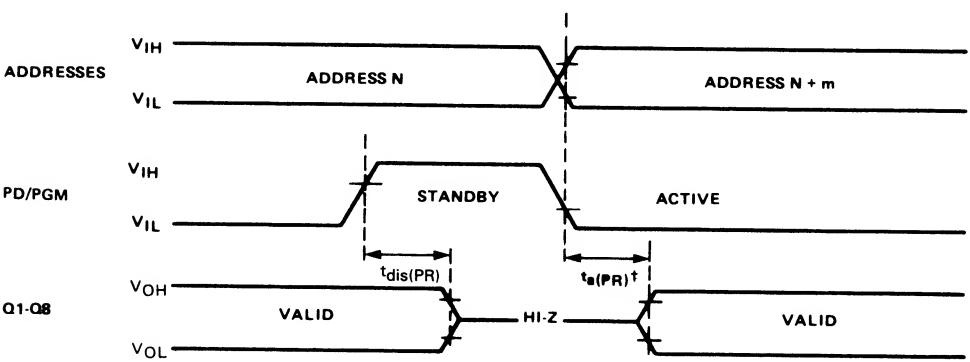


FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

read cycle timing



standby mode



NOTE: $\overline{CS}$ must be in low state during Active Mode, "Don't Care" otherwise.
$\dagger t_{a(PR)}$ referenced to PD/PGM or the address, whichever occurs last.

All timing reference points in this data sheet (inputs and outputs) are 90% points.

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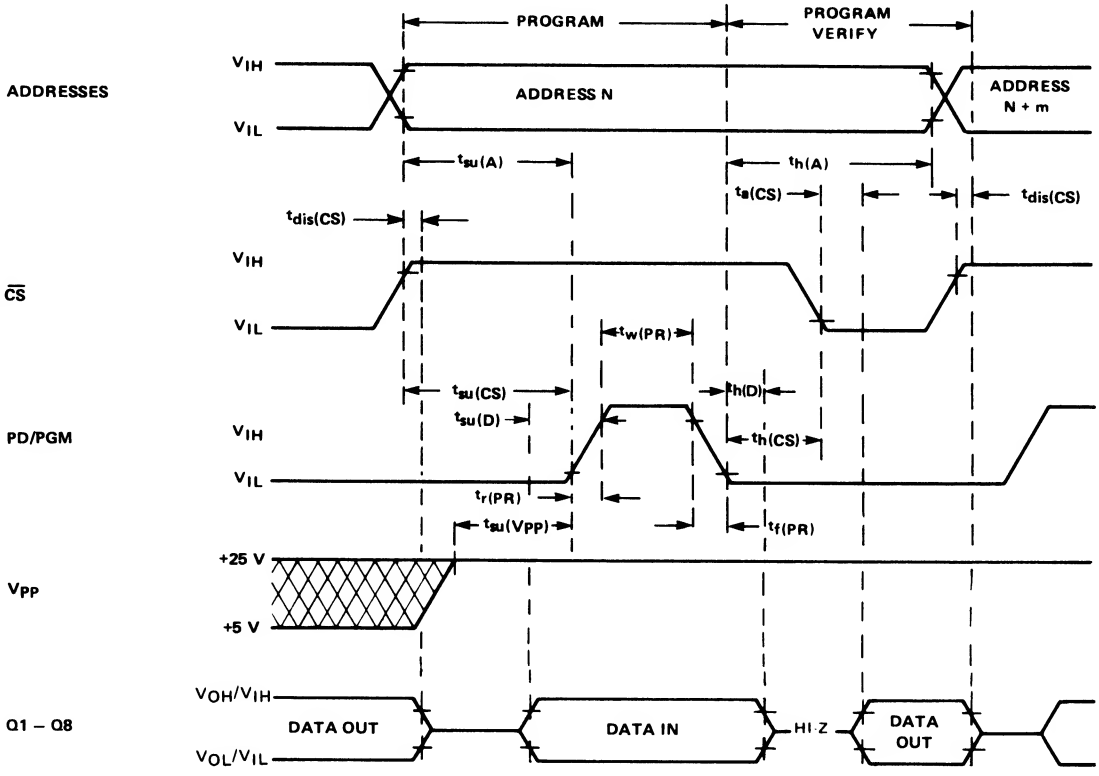
program cycle timing



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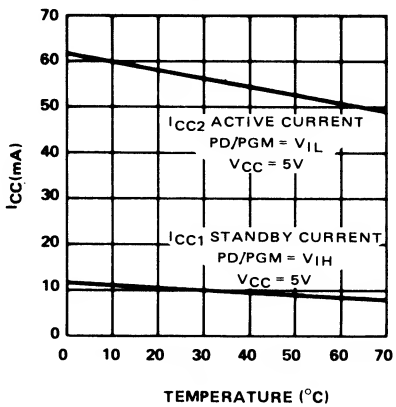
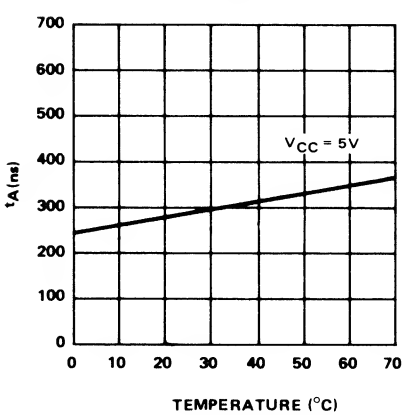
typical device characteristics (read mode)

TMS 2516-45
TMS 2516-35
TMS 2516-25
I_{CC} CURRENT
vs
TEMPERATURE



TMS 2516-45
TMS 2516-35
TMS 2516-25
ACCESS TIME
vs
TEMPERATURE



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